

Amendment under 37 CFR § 1.111  
Serial No. 10/807,327  
Attorney Docket No. 042271

**AMENDMENTS TO THE DRAWINGS**

The attached replacement sheets of drawings include changes to Figs.10-12 as attached.

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## **REMARKS**

### **Specification**

**The title of the invention was objected to as not being descriptive.**

Accordingly, the title has been amended to become descriptive.

**The specification was also objected to as failing to provide proper antecedent basis for the claimed subject matter.**

Accordingly, the specification has been amended to overcome the objection.

Fig. 2 shows a layout illustrating a configuration of a semiconductor device (ferroelectric memory) according to the first embodiment of the present invention, in which a straight line connecting the source and the drain of the transistor extends in a direction substantially inclined at an angle of 45 degrees to the longitudinal and lateral directions of the array constituted by the plurality of ferroelectric capacitors. Fig. 2 also shows that the line connecting the source and the drain of one of the two transistors substantially coincides with the line connecting the source and the drain of the other one of the two transistors.

Also, Fig. 6 shows a layout illustrating a configuration of a semiconductor device (ferroelectric memory) according to the second embodiment of the present invention, in which the line connecting the source and the drain of one of the two transistors is substantially orthogonal to the line connecting the source and the drain of the other one of the two transistors.

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Thus, the specification as amended provides proper antecedent basis for the claimed subject matter.

### **Drawings**

**The drawings were objected to as failing to comply with 37 CFR 1.84(p)(5) because they include reference characters not mentioned in the description.**

Reference numeral 33 appears on page 13 as “contact hole 33.” Reference numeral 10 appears on page 12 as “W plug 10.”

As to other objected reference numerals, most of reference numerals are deleted from Figs 10 to 12.

**The drawings were objected to as failing to comply with 37 CFR 1.83(a).**

The Examiner alleged that the drawings do not show (a) the line connecting the source and the drain of one of said two transistors substantially coincides with the line connecting the source and the drain of the other one of said two transistors; (b) the line connecting the source and the drain of one of said two transistors is substantially orthogonal to the line connecting the source and the drain of the other one of said two transistors; and (c) extends in a direction substantially inclined at an angle of 45 degrees to longitudinal and lateral directions of the array constituted by the plurality of ferroelectric capacitors.

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The specification has been amended to specify the drawings which show these recited features. A person of ordinary skill in the art would clearly understand the recitations are shown in the drawings. As already discussed, Fig. 2 shows a layout illustrating a configuration of a ferroelectric memory according to the first embodiment of the present invention, in which a straight line connecting the source and the drain of the transistor extends in a direction substantially inclined at an angle of 45 degrees to the longitudinal and lateral directions of the array constituted by the plurality of ferroelectric capacitors. Fig. 2 also shows that the line connecting the source and the drain of one of the two transistors substantially coincides with the line connecting the source and the drain of the other one of the two transistors.

Also, Fig. 6 shows a layout illustrating a configuration of a semiconductor device (ferroelectric memory) according to the second embodiment of the present invention, in which the line connecting the source and the drain of one of the two transistors is substantially orthogonal to the line connecting the source and the drain of the other one of the two transistors.

The description in the specification has been amended to make a person of ordinary skill in the art clearly understand that the claimed recitations are shown in the drawings.

### **Claim Objections**

**Claims 5 and 6 were objected to because of the informalities.**

Claim 6 has been amended to overcome the objection. Claim 5 has been cancelled to make the objection moot.

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### **Information Disclosure Statement**

**The Information Disclosure Statement filed March 24, 2004 allegedly failed to comply with 37 CFR 1.98(a)(2).**

The reference submitted in the IDS, PATENT ABSTRACTS OF JAPAN 2003092391 is not more material than the references cited in the prior art rejection in the Office Action, but it was cited to show a level of the technical field. The Examiner objected to because only the Abstract was submitted without a copy of the entire patent application. A copy of the publication of the entire patent application is submitted herewith.

### **Rejections under 35 USC §112, Second Paragraph**

**Claims 2-12 were rejected under 35 USC §112, second paragraph, as being indefinite because what is meant is allegedly unclear by (a) “located at substantial central point of a minimal rectangular shape made by four ferroelectric capacitors out of said plurality of ferroelectric capacitors.” and (b) “located at substantial central point of a minimal rectangular shape made by four ferroelectric capacitors out of said plurality of ferroelectric capacitors.”**

Accordingly, the claims have been amended for clarification.

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Regarding (a), the corresponding recitation has been amended to “substantially located in a center of an area surrounded by four closest ferroelectric capacitors out of said plurality of ferroelectric capacitors.”

Regarding (b), claims 1 and 2 have been amended to recite “said plurality of ferroelectric capacitors are arranged in an array extending in longitudinal and lateral directions” giving clear definition to the longitudinal and lateral directions.

#### **Rejections under 35 USC §102(e)**

**Claim 1 was rejected under 35 USC §102(e) as being anticipated by Summerfelt et al. (U.S. Patent Publication No. 2005/0012125).**

Claim 1 has been cancelled making the rejection moot.

#### **Rejections under 35 USC §102(a)**

**Claim 2 was rejected under 35 USC §102(a) as being anticipated by Applicant's Prior Art.**

Claim 2 has been amended to recite “wherein the second contact plug is substantially located in a center of an area surrounded by four closest ferroelectric capacitors out of said plurality of ferroelectric capacitors.”

In Figure 10 of the present application, the second contact plug is located in the middle between two closest ferroelectric capacitors, but NOT “substantially located in a center of an area

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surrounded by four closest ferroelectric capacitors out of said plurality of ferroelectric capacitors.”

For at least these reasons, claim 2 patentably distinguishes over Applicant’s Prior Art.

**Rejections under 35 USC §103(a)**

**Claims 3, 5 and 9 were rejected under 35 USC §103(a) as being obvious over Summerfelt et al. (U.S. Patent Publication No. 2005/0012125).**

Claims 3, 5 and 9 have been cancelled to make the rejection moot.

**Claim 4 was rejected under 35 USC §103(a) as being obvious over Applicant’s Prior Art.**

Claim 4 depends from claim 2. As discussed above, claim 1 patentably distinguishes over Applicant’s Prior Art.

For at least these reasons, claim 4 also patentably distinguishes over Summerfelt for at least the same reasons.

**Claims 6 and 10 were rejected under 35 USC §103(a) as being obvious over Applicant’s Prior Art in view of Summerfelt et al. (U.S. Patent Publication No. 2005/0012125).**

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Claims 6 and 10 indirectly depend from claim 1. As discussed above, Claim 2 patentably distinguishes over Summerfelt.

For at least these reasons, claims 6 and 10 also patentably distinguish over Summerfelt for at least the same reasons.

**Claims 7 and 11 were rejected under 35 USC §103(a) as being obvious over Summerfelt et al. (U.S. Patent Publication No. 2005/0012125) in view of Corvasce et al. (U.S. Patent No. 6,656,801).**

Claims 7 and 11 have been cancelled to make the rejection moot.

**Claims 8 and 12 were rejected under 35 USC §103(a) as being obvious over Applicant's Prior Art in view of Summerfelt et al. (U.S. Patent Publication No. 2005/0012125) and Corvasce et al. (U.S. Patent No. 6,656,801).**

Claims 8 and 12 indirectly depend from claim 2. As discussed above, Claim 2 patentably distinguishes over Applicant's Prior Art.

Summerfelt et al was cited for allegedly disclosing a semiconductor device which has an element isolation insulating film formed on the surface of said semiconductor device and isolating plurality of element regions, wherein each element region includes two transistors out of said plurality of transistors.



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Corvasce et al was cited for allegedly disclosing a semiconductor device which has the line connecting the source and the drain of one of the two transistors is substantially orthogonal to the line connecting the source and the drain of the other one of the two transistors.

Such disclosures of Summerfelt et al and Corvasce et al, however, do not remedy the deficiencies of Applicants' Prior Art discussed above.

For at least these reasons, claims 8 and 12 also patentably distinguish over Applicants' Prior Art, Summerfelt and Corvasce et al.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

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If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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Enclosures: Supplemental IDS

Replacement Sheets for Figs. 10-12

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